
Lumache

Release 0.1

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This is mostly a blog with a documenting style since it will mostly describe specific information about HDL and FPGA

Note: This project is under active development.

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1.1 Packages in VHDL

1.1.1 Package

In addition to a testbench-files and regular synthesis-files VHDL provides library-files called **packages**. Package is a usefull file to collect some universal data so it would not increase the size of the design files. This kind of files is desribed by VHDL LRM and must be supported with all vendors. I've checked it with:

- Quartus 18.0
- Modelsim 10.5
- Vivado/Vsim 2019.2
- All edaplayground.com instruments

1.1.2 Synthax

The synthax an be seen in the ieee library: `numeric_std`, `std_logic_1164` are also packages.

Package file consists of 2 main parts: the package itself and package body:

```
package my_pkg is  
  
end package my_pkg;  
package body my_pkg is  
  
end package body my_pkg;
```